SPECIFICATION AMENDMENTS:

Please replace the paragraph on page 2, lines 14 through 20, with the following amended paragraph:

-- However, since each of the bump electrodes is erected from the uppermost layer wiring as described above, it is impossible to make longer the bump electrode longer without changing a-the thickness of the whole semiconductor device. Further, there has been a problem that for reducing the thickness of the whole semiconductor device or increasing the number of layers of the wiring of the CSP structure without changing the thickness thereof, the height of the bump electrode should be shortened contrariwise. --

Please replace the paragraph on page 4, lines 19 through 27, with the following amended paragraph:

--The wiring patterns 12a, 12b, ··· are made of the second wiring layer material. These patterns are referred to as redistribution wirings. Particularly, the second wiring pattern is also called as second level wiring pattern. The second wiring layer is also called as-a_second level wiring layer._Among wiring patterns 12a, 12b, ··· of the second wiring layer 12, the predetermined wiring pattern has depressed portions 20. The depressed portions 20 are formed in positions of the via holes 13 and 15. The second wiring patterns are electrically connected individually to the predetermined wiring patterns of the first wiring layer 7.--

AMENDMENT 10/714,962

Please replace the paragraph on page 10, lines 7 through 15, with the following amended paragraph:

-- Further, the third insulating layer 16 (the upper most insulating layer) covers the second wiring layer 12 and the second insulating layer 10 having different adhesion tendencies relative to the sealing resin layer 17, and the concave portions formed around the bump electrodes 14 in the leveled state. With this structure, the filler material having a relatively large particle size and included in the sealing resin layer 17 does not enter into the concave portions. As a result, this structure can be kept uniform in the adhesion degrees states at various portions without forming voids, so that it becomes possible to improve moisture resistance of the semiconductor device. --

Please replace the paragraph on page 12, line 26 through line 31, with the following amended paragraph:

-- Each bump electrode 35 is formed by plating so as to cover the depressed portion 38. Thereupon, for example, a resist-recess is formed such that a bump space having the depressed portion 38 as a bottom portion thereof is formed, and plating is implemented to form the bump electrode 35 in the bump space, so that, as shown in Fig. 2, the bump electrode 35 is formed such that the shape of its cross section covers the area of the depressed portion 38. --

AMENDMENT 10/714,962

DRAWINGS AMENDMENTS:

Fig. 1 has been changed to correct an error in the leader line of reference number 4, the surface protective film, that was incorrectly identifying the first insulating layer 5.

AMENDMENT

10/714,962